In re Patent Application of:
SFERRAZZA ET AL
Serial No. **10/686,362**
Filed: **OCTOBER 15, 2003**

IN THE SPECIFICATION:

Please replace paragraph [0007] beginning at page 4, with the following rewritten paragraph:

[0007] During normal operation or 'RUN'/'ACTIVE' mode, some charge is stored across an RC filter capacitor 31 as the feedback loop through the error amplifier 10 supplies a control input to the PWM driver circuitry 20. When the power supply transitions from active mode to 'SLEEP'/'QUIESCENT' mode, however, this charge begins to bleed off or discharge through the filter's resistor circuitry, as the normal operation of the error amplifier 10 and the PWM circuit [30]20 is temporarily interrupted. Eventually, when the power supply transitions out of QUIESCENT mode and back into RUN mode, the discharged capacitor 31 will take some finite amount of time to recharge as the PWM driver circuitry 20 is again active. During this interval, the output node 43 provides a voltage that is different from the correct value and appears to downstream powered devices as a power rail anomaly, which can cause misoperation of one or more devices.

Please replace paragraph [0016] bridging pages 8-9, with the following rewritten paragraph:

[0016] Attention is now directed to Figure 3, wherein the sample and hold-based, voltage compensation circuit 60 of Figure 2 is diagrammatically illustrated as comprising a binary counter 300, that is sequentially incremented by a clock signal ~~'clk'~~ 'CLK' and is reset by reset signal ~~'rst'~~ 'RST' supplied by way of the converter's control circuitry. Outputs of respective stages of binary counter 300 are coupled to associated inputs of current mirror stages within a multistage current mirror 310, such as may be referenced to a bandgap voltage source. The currents produced

by multistage current mirror 310 are summed through a summing resistor 320, which is coupled to a first, non-inverting (+) input 341 of a 'compensation' differential amplifier 340. A second, inverting (-) input 342 of compensation amplifier 340 is coupled to a compensation pin COMP, which corresponds to the output node 13 of Figure 2, to which the AC compensation filter 30 of error amplifier 10 is coupled. The respective stages of binary counter 300 are coupled by means of a set of combinational logic ~~gate~~ to the gate 351 of a sample and hold FET 350, which has its source-drain path 352-353 coupled in circuit with a resistor 360 installed in a feedback path of compensation amplifier 340. A disable input ~~'dis'~~ 'DIS' is coupled from control circuitry to the amplifier 340. The ~~'dis'~~ 'DIS' input is used to disable the amplifier in RUN mode; when the disable input ~~'dis'~~ 'DIS' is removed during SLEEP mode, amplifier 340 is enabled.

Please replace paragraph [0017] beginning on page 9, with the following rewritten paragraph:

[0017] In operation, in response to a RUN-to-SLEEP mode transition of the power supply circuit, the disable input ~~'dis'~~ 'DIS' to compensation amplifier 340 is removed, as described above, and a reset input ~~'rst'~~ 'RST' is applied from the controller to the binary counter 300 to clear its contents. Counter 300 then begins being sequentially incremented by the clock signal ~~'clk'~~ 'CLK'. As the counter 300 is incremented, associated current mirror stages of the multistage current mirror 310 sequentially increment the amount of current being summed through resistor 320. When the magnitude of the currents summed through resistor 320 produce a voltage thereacross that equals the value of the compensation voltage V_{comp} at the compensation node COMP, the output of amplifier 340 is tripped and changes state.

In re Patent Application of:
SFERRAZZA ET AL
Serial No. **10/686,362**
Filed: **OCTOBER 15, 2003**

Please replace paragraph [0018] bridging pages 9-10, with the following rewritten paragraph:

[0018] This change in state of the output of amplifier 340 is coupled to the counter 300 over link 343 to terminate operation of the counter and thereby effectively 'freeze' its count value. In response, counter 300 couples an output over link 301 to the gate of FET 350 to place amplifier 340 in a unity gain state, so that the voltage at the compensation pin COMP is maintained at its 'frozen' value. The compensation voltage V_{COMP} at the COMP node is maintained during SLEEP mode ~~back~~, and is thus immediately available to the PWM driver circuitry 20, so that the problem of charge bleed off from in the AC compensation RC filter 30 is obviated, and a smooth transition between SLEEP and RUN mode is afforded. When the converter returns to RUN mode, the disable input ~~'dis'~~ 'DIS' is again applied to amplifier 340, and the sample and hold circuitry becomes inactive, waiting for an assertion of SLEEP mode of operation, as described.